Amendments to the Specification

Please replace the paragraph beginning at page 3, line 16, with the following rewritten paragraph:

For optimal performance of turbo equalization, the coded bits also should be sufficiently interleaved in transmission. The interleaving serves two purposes. On one hand, it can effectively eliminate the correlation among soft-messages associated with coded bits of small distance in the block structure for decoding purposes. On the other hand, interleaving can eliminate the dependence among the ~~messages~~ soft values feed back to the same coherent block for demodulation. A commonly conceived interleaving structure is *random* interleaving. To achieve random interleaving, however, the same (randomly generated) permutation must be accessible, e.g., stored, at both the transmitter and the receiver. This inflicts large memory requirements for practical systems coded by large block codes.

Please replace the paragraph beginning at page 6, line 5, with the following rewritten paragraph:

Figure 7 illustrates the correspondence between soft values from the LDPC decoder and the transmission units using the exemplary code structure shown in Fig.3. The soft values include ~~3 bits~~ 3 bits.

Please replace the paragraph beginning at page 6, line 15, with the following rewritten paragraph:

The present invention is directed to methods and apparatus for data communication over a block-coherent channel. For simplicity, we refer to the symbols transmitted in one coherent interval as a *dwell*. The length of a dwell is L. The symbols of a dwell, serve as an information transmission unit, that includes M information symbols and (L-M) known symbols. Each information symbol is a symbol mapped from ~~P bit(s)~~ P bit(s) in a codeword.

Please add the following new paragraph beginning at page 8, line 3, before the paragraph beginning "The vectorized encoding process":

Coded bits are stored in memory configured as Z x n. Or equivalently, we view the binary codeword as n Z-vectors, each vector including Z bits. The Z used in vector LDPC codes is a multiple of P, the number of bits associated with a transmitted symbol. For assumed QPSK modulation where P=2, we have $Z=2z$, where z is the number of symbol's-worth of bits in a Z-vector. We further select the number of columns to be a multiple of M, the number of information transmission symbols in a transmission unit, i.e. $n=qM$.

Please replace the paragraph beginning at page 8, line 4, with the following rewritten paragraph:

The vectorized encoding process, as described in the U.S Patent 6,961,888 ~~Application S.N.~~ _____ titled "METHODS AND APPARATUS FOR ENCODING LDPC CODES" filed July 11, 2003, may arrange these columns such that the degrees of their associated variable nodes are in an increasing order. Such an ordering facilitates an algebraic interleaving method that

forms dwells with coded bits associated with variable nodes of wide range of degrees. An exemplary way is to uniformly divide the matrix into M=t-1 contiguous sub-matrices. The property that columns are ordered in increasing degree ensures that the sub-matrices contain variable nodes of similar degrees: the first sub matrix has the lowest degree, the last sub matrix the highest. Thus a dwell formed by taking two bits from different sub-matrices has the desired property.

Please replace the paragraph beginning at page 8, line 18, with the following rewritten paragraph:

An exemplary interleaver apparatus of the invention includes a memory for storing coded bits and an interleaving circuit. The interleaving circuit generates a set of control information which is used to control the reading of bits from the memory. Each set of generated control information includes a transmission unit identifier, a Z vector identifier, and a row identifier. The control circuit, in an exemplary embodiment, includes four components: a symbol ID generation module, a bits ID generation module, a column ID generation module and a control information generator module. The symbol ID generation module may be implemented as a repeating counter that generates a number *s* ranging from 0 to M-1. The repeating counter is incremented periodically as a function of a system clock *clk*, e.g., *s* is incremented once per clock cycle; the number *s* determines the symbol index in a dwell. The bits ID generation module may also be implemented as a repeating counter, e.g., a repeating counter generating a number *b* ranging from 0 to z-1. The number *b* is periodically incremented each time the symbol index signal *s* reaches zero; number *b* determines the bits index ~~selected~~ in a ~~the column~~

selected column, e.g., a ~~row of the c column in an array which is stored in memory~~. Column ID generation module 603 generates a number c ranging from 0 to a-1 and may be implemented as another counter. The number c is incremented each time the bits index b reaches zero; number c is the column index. Taking bits index b, symbol index s, and column index c, a control information generator module produces a set of control information including a transmission unit identifier, a Z vector identifier and a row identifier used to control which location in the coded bits memory is accessed. In one exemplary embodiment, the Z-vector identifier is c + a x s, and the row identifier is Z x b. The transmission unit is identified by a transmission unit identifier having the value b+cxZ, where b and c are as defined above and where Z is the number of elements in each Z vector and where x indicates a multiplication operation.

Please replace the paragraph beginning at page 9, line 9, with the following rewritten paragraph:

At the receiver side, the direct mapping between data bits and transmission units is conformed for demodulation. It is assumed that soft-outputs from the decoder have the same ordering as the binary code word structure. The soft values includes, however, K-bits corresponding to a coded bit. Each of k bits may be stored in a different one of D arrays in memory where D is a positive integer. In most cases, ~~k~~ K is an integer multiple of D. One exemplary memory has three-bit soft values for each bit, each identified by the same code bit identifier. Those three bits might be in one memory location; or those three bits could be in three different memory location. With this structure, it

is clear that the same type of interleaving apparatus used in a transmitter can also be used in a receiver to access soft values corresponding to a transmission unit for purposes of demodulation.

Please replace the paragraph beginning at page 10, line 30, with the following rewritten paragraph:

~~Coded bits are stored in memory configured as Z x n. Or equivalently, we view the binary codeword as n Z-vectors, each vector including Z bits. The Z used in vector LDPC codes is a multiple of P, the number of bits associated with a transmitted symbol. For assumed QPSK modulation where P=2, we have Z=2s. We further select the number of columns to be a multiple of M, the number of information transmission symbols in a transmission unit, i.e. n=aM.~~ An interleaving method of the invention determines the location of the Z bits associated with each symbol in each transmission unit. Clearly, the memory location corresponds to a Z-vector identifier and the ~~offset value~~ bit index inside the Z-vector. The present invention orders coded data as follows: The jth dwell (where j is from ~~1~~ 0 to z x a-1) will contain Zbits *in the Z* ~~bit~~ *vector identified by* ~~i + a/M + [j/(Z/P)] [j/s] + a * i~~ *with* bit index ~~offset value~~ *2* (j mod Z/P)*, where i is from 0 to *M-1*. In such a case, the address used to retrieve the data bits can be easily generated algebraically, without the use of memory for this purpose.

Please replace the paragraph beginning at page 12, line 5, with the following rewritten paragraph:

An apparatus, e.g., interleaver 102 of the invention, for the proposed interleaving technique is shown in Fig. 6. The interleaver 102 includes a memory 610 for storing coded bits and an interleaving circuit 600 coupled together as shown in Fig. 6. Interleaving circuit 600 generates a set of control information which is used to control the reading of dibits from the memory 610. Each set of generated control information includes a transmission unit identifier, a ~~Z-vector~~ Z vector identifier, and a row identifier. Circuit 600 includes four components: a symbol ID generation module 601, a bits ID generation module 602, a column ID generation module 603 and a control information generator module 604. Module 601 is a repeating counter that generates a number *s* ranging from 0 to M-1. The counter 601 is incremented periodically as a function of a system clock *clk*, e.g., *s* is incremented once per clock cycle; number *s* determines the symbol index in a dwell. Module 602 is a repeating counter generating a number *b* ranging from 0 to *z*-1. The number *b* is periodically incremented each time the symbol index signal *s* reaches zero; number *b* determines the bits index ~~selected~~ in a selected ~~the~~ column, e.g., the bit index *a* row of ~~the~~ a column in array 600 which may be stored in memory 605. Module 603 is another counter. Module 603 generates a number *c* ranging from 0 to *a*-1. The number *c* is incremented each time the bits index *b* reaches zero; number *c* is the column index. Taking bits index *b*, symbol index *s*, and column index *c*, a control information generator module 604 produces a set of control information including a transmission unit identifier, a Z-vector identifier, and a row identifier used to control which location in the coded bits memory 605 is accessed. The Z-vector identifier is $c + a \times s$, and the row identifier is $2 \times b$. The transmission unit is identified by a transmission unit

identifier having the value b*cxZ, where b and c are as defined above and where Z is the number of elements in each Z-vector and where x represent a multiplication operation.

Please replace the paragraph beginning at page 12, line 14, with the following rewritten paragraph:

At the receiver side, the direct mapping between data bits and transmission units is conformed for demodulation. We assume that soft-outputs from the decoder have the same ordering as the binary code word structure, e.g., as shown in array 600. The soft values includes, however, K bits corresponding to a coded bit. Each of * K bits may be stored in a different one of D arrays where D is a positive integer. In most cases, * K is an integer multiple of D. An exemplary memory 700 has three-bit soft values for each bit, each identified by the same code bit identifier. Those three bits might be in one memory location; or those three bits are in three different memory location 701, 702, 703, as shown in 700. With this structure, it is clear that the same interleaving circuit 600 can be used to access soft values for a transmission unit for demodulation.

Please replace the paragraph beginning at page 13, line 21, with the following rewritten paragraph:

~~Many of the~~ The above described method ~~methods or~~ and method steps can be implemented using machine executable instructions, such as software, included in a machine readable medium such as a memory device, e.g., RAM, floppy disk, etc.

to control a machine, e.g., general purpose computer with or without additional hardware, to implement all or portions of the above described methods, e.g., in one or more communications network nodes. Accordingly, among other things, the present invention is directed to machine-readable medium including machine executable instructions for causing a machine, e.g., processor and associated hardware, to perform one or more of the steps of the above-described method ~~method(s)~~.